A METHOD OF REDUCING DELAYS

ABSTRACT

A method is described for reducing delays in an analogue simulation model of a hardware circuit. The method includes ~~comprises~~ the steps of stimulating via an input an output of said analog ~~analogue~~ model, said output and said input having a relatively high resistance therebetween and applying a pulse to a relatively low resistance, whereby when said pulse is applied to the relatively low resistance, the input is connected to said output via the relatively low resistance so that the time constant of the circuit is reduced.